The Examiner relied on the Penna patent as teaching the polygon rendering which includes mapping of texels from a texture map onto pixels within the polygon.

The rejection is being herein respectfully traversed.

The admitted prior art shows in Fig. 3 an array of pixel data, considered as the source frame image data and in fig. 5 an array of pixel data as destination pixel data. Convolution filtering is performed sequentially for each pixel in each row of the array.

No rendering means or step wherein the action of applying a stipulated pixel-unit operation to the source image data stored in the first storage means and rendering the data as destination image data in the second storage means of the image processing device is performed in units of polygons is performed repeatedly until a stipulated arithmetic result is obtained is suggested in the AAPA.

Penna teaches a graphic image rendering method and apparatus for polygon rendering in two dimensional screen space, which use a storage (20) for calculated polygon edge data to enable continuous edges to be maintained over at least two rendering windows.

In Penna, the steps of rendering the part of the polygon lying within the rendering window by mapping texels from the texture map and moving the rendering window to a further position within the two dimensional screen space overlying at least a part of the polygon and abutting a previous rendering window positions are sequentially repeated until all of the polygon has been rendered. The texture map holds fewer texels that are required to render a full screen. The first rendering window overlies a vertex of the polygon and slope values for the polygon edges to the vertex are calculated and stored, an intercept point on one of each edge is identified to sub-pixel accuracy and stored, and for each further rendering operation where a rendering

window overlies a part of one or other of the polygon edges, the previously calculated slope values and intercept point locations are recalled from storage.

Penna et al., for each polygon executes the steps of:

defining a texture rendering window covering a number of pixels requiring, in total, less than or equal to the number of texels in a texture map for rendering;

determining the vertical height of the uppermost vertex of the polygon within said two dimensional screen space and positioning the rendering window such that it overlies at least a part of the polygon and the uppermost extent of the window is at or above the vertical height of said uppermost vertex of the polygon;

rendering that part of the polygon lying within said rendering window by mapping texels from the texture map; and

moving said rendering window to a further position within said two dimensional screen space overlying at least a part of said polygon and abutting a previous rendering window position;

the rendering and moving steps are sequentially repeated until all of the polygon has been rendered. The texture map hold fewer texels than are required to render a full screen and the first rendering window overlies a vertex of polygon and slope values for the polygon edges to the vertex are calculated and stored, an intercept point on one of each edge is identified to sub-pixel accuracy and stored, and for each further rendering operation where a rendering window overlies a part of one or other of the polygon edges, the previously calculated slope values and intercept point locations are recalled from storage.

No rendering windows are required or claimed in the applicant's invention.

Penna et al as well as AAPA fail to suggest means for or a step of rendering in which a stipulated pixel-unit operation is applied to the source image data stored in the first storage means and the data are rendered as destination image data in the second storage means in units of polygons repeatedly until stipulated arithmetic result is obtained.

Moreover, a skilled artisan would not find any hint in the Penna et al disclosure to suggest him to use a rendering operation as claimed in the applicant's claims.

Thus claims 1, 8 and 9 as well as the claims respectively dependent thereon are not believed to be obvious from the combination of AAPA and Penna et al.

Claims 1,8-10,17-19 and 26-27 are rejected under 35 U.S.C. § 102(e) as being anticipated by Okada (6,151,035). It is to be noted that both the Okada patent and the present application have the same assignee.

Okada discloses a two-buffer graphic data display with a graphic data generation circuit, a frame memory and a display. The graphic data generation circuit performs reduction processing during a display-blanking period of the display device.

The Examiner refers to col. 4, line 61 to col. 5, line 9 of the Okada disclosure as teaching rendering the data as destination data in the second storage means in units until a stipulated arithmetic result is obtained.

According to Okada, the main CPU 44 controls the CD-ROM drive 56, reads application programs data and sound, image and parameter data from the CD-ROM 40 on the CD-ROM drive 56 and stores these data in the main memory 45. The main CPU 44 and first vector processing engine 71 perform processing which requires fine operation in polygon unit which is (as Okada specifies) one of the geometry processing.

The Examiner also states that Okada discloses an action of stipulated pixel-unit operation to the source image data in units of polygons and referred to Fig. 7 of the reference.

As disclosed in col. 6, line 43 to col. 7, line 53 Okada suggests that his unit is a pixel. No reference to units of polygons could be found in the Okada disclosure.

It is therefore believed that the rejection of claims 1, 8-10, 17-19, 26-27 under 35 U.S.C. § 102 is not an appropriate rejection.

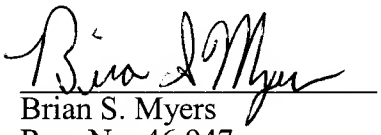
In view of the foregoing it is respectfully submitted that claims 1-27 are allowable over the prior art.

Attached hereto is a marked-up version of changes made to the claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**."

Any fee due with paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Reconsideration and allowance is most respectfully solicited.

Respectfully submitted,



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## Version with Markings to Show Changes Made

IN THE SPECIFICATION

The paragraph at page 2, lines 7-11 was replaced with the following paragraph:

In step S1, CPU 5 receives a supply of image data corresponding to one frame from video camera 1. This image data, which can be considered as the source frame image data, consists of an HMAX, VMAX array of pixel data $C_{SF}$ as shown, for example, in Fig. 3. In step S1, CPU 5 also sets the convolution filter coefficients $C_v[m][n]$. In the Example in Fig. 4, these convolution filter coefficients $C_v[m][n]$ consist of a 3x3 array of coefficients.